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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,144	10/31/2003	Douglas D. Boom	5038-331	2967

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EXAMINER	
KIM, KENNETH S	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,144	BOOM ET AL.	
	Examiner	Art Unit	
	Kenneth S. KIM	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

KENNETH S. KIM
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Jan20'04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-15, 17-23, and 25-28 are presented for examination.

2. The abstract of the disclosure is objected to because the current abstract is too long (over 250 words). Correction is required. See MPEP § 608.01(b).

3. Applicant is requested to describe what is p-code in the specification.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-15, 17-23, and 25-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(a) Claim 1, it is not clear what is meant by "concurrent in-line stating (or staging)".

(b) Claim 14, it is not clear what is meant by "p-code".

(c) Claim 14, "retiring instructions back to instruction cache" is ambiguous as to what instructions it is referring to and as to what is meant by *retiring back,* since the instructions already in the cache.

(e) Claim 22, it is not clear what is the utility of detecting an impending natural context switch.

(f) Claim 25, the origin of decode micro-opcodes representing interrupt servicing instructions is ambiguous.

(g) Claim 28, the same as (a), and "the executed micro-opcodes" lacks antecedent basis.

Note: Upon clarification, some groups of claims may be subject to restriction requirement.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 5-9, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Arora et al, U.S. Patent No. 6,625,693.

Arora et al teaches the invention as claimed in claim 1 including a method comprising:

(a) detecting an interrupt service request (hardware signal for exception; col. 3, line 35),

(b) inserting interrupt servicing instructions into an instruction queue mechanism (cache and fetch; col. 3, line 51) in response to detecting the interrupt service request where inserting the interrupt servicing instructions into the instruction queue mechanism result in processor bandwidth being allocated between the inserted interrupt servicing instructions and other program instructions (the processor executes instructions in sequence, thus allocating bandwidth) via concurrent in-line stating of the interrupt servicing instructions and other program instructions,

(b) executing the interrupt servicing instructions and other program instructions. (105), and

further teaches as in claims 2, 5-9,

(c) the instruction queue mechanism includes an instruction cache (101) and an instruction fetch unit to fetch instructions from the instruction cache, the processing being performed in such manner as to decode the instructions into micro-opcodes (firmware) and execute the micro-opcodes in one or more out-of-order execution units (col. 3, line 31) – claim 2, and

(e) dynamically detecting comprises detecting plural interrupts by prioritizing the plural interrupts and inserting one or more instances of the interrupt servicing instructions into the instruction queue mechanism in accordance with one or more predefined interrupt servicing allocation criteria and capacity (col. 3, line 53) without flushing the instruction queue mechanism (not flushed) – claims 5-9.

The processor claims 11 and 12 are equivalently rejected based on the same reason.

8. Claims 1–4 are rejected under 35 U.S.C. 102(b) as being anticipated by Crump et al, U.S. Patent No. 5,557,759.

Crump et al teaches the invention as claimed in claim 1 including a method comprising:

(a) detecting an interrupt service request (col. 18, line 22),

(b) inserting interrupt servicing instructions into an instruction queue mechanism (cache and fetch) in response to detecting the interrupt service request where inserting the interrupt servicing instructions into the instruction queue mechanism (col. 18, lines 24 and 34) result in processor bandwidth being allocated between the inserted interrupt

servicing instructions and other program instructions (the processor executes instructions in sequence, thus allocating bandwidth) via concurrent in-line stating of the interrupt servicing instructions and other program instructions,

(b) executing the interrupt servicing instructions and other program instructions. (30), and

further teaches as in claims 2-4,

(c) the instruction queue mechanism includes an instruction cache (31; col. 14, line 46) and an instruction fetch unit to fetch instructions from the instruction cache, the processing being performed in such manner as to decode the instructions into micro-opcodes (30, col. 3, line 24) and execute the micro-opcodes in one or more out-of-order execution units (superscalar machine) – claim 2,

(d) recycling the executed micro-opcodes for optional re-execution thereof in the one or more out-of-order execution units by retiring the executed micro-opcodes including those micro-opcodes representing the inserted interrupt servicing instructions to the instruction cache in order (col. 14, line 51) – claims 3 and 4.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sturges taught a method of allocating processor resource to processes including ISR.

Witt et al taught a superscalar processor executing micro-codes out-of-order.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (571) 272-3627. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

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December 16, 2005

KENNETH S. KIM
PRIMARY EXAMINER